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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,005	09/09/2002	Vinod Nair Gopikuttan Nair	2000P17005US	3747

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,005	NAIR ET AL.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 23 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Klingman (US5541930).

1. As to claims 1,9, and 23,Klingman discloses an interface unit and method for communication between an integrated services digital network (ISDN) based bus and a processor bus, wherein data in the ISDN-based bus is transferred in ISDN frames divided into a plurality of slots comprising: (Klingman teaches of a interface unit 80 of figure 7 between an ISDN based bus 106, and a processor bus 102, where data is transferred in ISDN frames (50) divided into a plurality of slots (62,52,60,56) as illustrated in figure 4)

a data transfer unit includes a processor bus interface coupled to a processor bus, the processor bus interface includes a processor buffer,

(Klingman teaches of processor bus interface 146 in figure 8, coupled to processor bus 102 . Said interface comprises a buffer, COL. 7 - 17)

An ISDN bus interface coupled to an ISDN-based bus interface includes an ISDN buffer (Klingman teaches of ISDN interface 164, a Siemens 2085 device of figure 9, that comprises an ISDN buffer, COL. 6, line 65 – COL. 7, line 3)
A control unit coupled to the data transfer unit for controlling the transfer of data between the processor bus and ISDN-based bus, wherein the interface unit is capable of accessing all slots in an ISDN frame (Klingman teaches of control unit 162 of figure 9 that controls the transfer of data between the processor bus 102 and the ISDN bus 106, COL. 7, lines 20 - 35).

2. As to claims 2 and 3, Klingman discloses a processor bus interface coupled to the ISDN-based interface via an interface buffer comprising a group of register banks, having a control input terminal (Klingman teaches in figure 8 of processor bus interface 146 , coupled to the ISDN-based interface 164 of figure 9. Coupling takes place via memory unit 160 of figure 9, comprising of a group of register banks in a dual port memory, COL. 6, lines 18 - 29).

3. As to claim 4, (Klingman discloses the interface unit wherein the ISDN buffer comprises one shift register for parallel/serial data conversion. (Klingman teaches that said buffer is a dual port memory that can be configured as a shift register to afford the parallel to serial configuration, COL. 12, lines 5 – 10).

4. As to claim 5, Klingman discloses the interface unit of wherein the processor bus interconnects a central processing unit, a memory unit and peripheral devices. (Klingman teaches in figure 7 of a computer comprising of elements detailed in figure 8, of a processor, 112, memory unit 110, and peripheral device connected through ISDN transceiver, COL. 5, lines 15 - 29).

Claims 6 – 8,10 - 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klingman, and further in view of Klingman (US6219736), hereinafter Klingman2.

As to claim 6, Klingman does not disclose a modular bus for coupling to voice, data and/or video devices. (However, Klingman2 teaches of said configuration in figure 17. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Klingman with Kilngman2 as Klingman2 provides a means of inexpensive byte alignment, COL. 2, lines 48 - 57).

5. As to claims 7 and 8, Klingman does not explicitly disclose the interface unit wherein said processor bus is connected to a high-speed data transfer unit. (However, Klingman2 teaches that the processor bus can be a USB or fire wire bus, COL. 1, lines 45 – 60, figure 17).

6. As to claim 10, Klingman discloses the interface wherein the control unit is programmed to determine the direction of data transfer and which slot or slots to

access. (Klingman teaches of the control unit determining of data transfer direction via interrupt signals 172 and 178. The dual port memories determine the slot selection, COL. 6, lines 18 - 35).

7. As to claims 11, 13,15,16, Klingman discloses the interface either operates in frame-based processing or in slot-based processing. (Klingman teaches of the interface using frame based processing, COL. 2, lines 23 - 33).

8. As to claims 12, and 14, Klingman discloses the interface wherein the data transfer unit comprises a memory module for buffering data that are to be transferred between the processor bus and the ISDN-based bus. (Klingman teaches of a data transfer unit comprising a memory module 160 of figure 9 for buffering data between said buses).

9. As to claim 17, Klingman discloses the interface wherein the data transfer unit comprises:

processor bus interface storage (PBIS) block coupled to the processor bus, wherein the PBIS includes a PBIS memory unit for storing data that are to be transferred to or received from the processor bus; (Klingman teaches of interface storage elements SC 196 of figure 10 that stores data, COL. 7, lines 60 – COL. 8, line 9).

10. As to claim 18, Klingman discloses the interface wherein the control unit comprises a control register block (CRB) coupled to the processor bus for receiving control information for programming the interface, wherein based on the information, the appropriate time slots and direction are selected for data transfer. (Klingman teaches of control register block 198 coupled to processor bus 212 that controls the programming of the interface, COL. 11, lines 9 – 20).

11. As to claim 19, Klingman discloses the interface of claim 17 wherein the data transfer unit further comprises an interface buffer (IB) coupled to the PBIS and IBIS, the IB provides intermediate buffering of data between the PBIS and the IBIS blocks. (Klingman teaches of interface buffer 174 of figure 5, which provides intermediate buffering, COL. 12, lines 12 – 25).

12. As to claims 20 and 21, Klingman discloses the interface wherein the IB comprises a plurality of register banks, each register bank comprising a plurality of registers to form a register stack. (Klingman teaches of the IB as illustrated in figure 10 that comprises a plurality of registers such as 1st TBUF, 2nd. T BUF, COL. 7, line 58 – COL. 8, line 20).

13. As to claim 22, Klingman discloses interface 9 wherein the control comprises a control register block (CRR) coupled to the processor bus for receiving control information for programming the interface, wherein based on the information, the

appropriate port time slots and direction are selected for data transfer. (Klingman teaches of a control register 162 of figure 9 that performs said functions, COL. 8, lines 20 - 34).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571 272 3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

CAD
9/01/2005